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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,751	01/26/2004	Leonard C. Pipes	ITL.0851D1US (P15016D)	8763

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,751	PIPES ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 22-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 22-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the after-final amendment and RCE filed on 8/29/05 and 11/14/05, respectively. Currently, claims 22-27 are pending.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/14/05 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 22-27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, in the amendment filed on 5/31/05, the newly added limitation, " higher etch rate" contains new matter not originally filed in the drawings, specifications and claims.

Additionally, see amendments filed after 5/31/05, where limitations regarding "etch rate" contain new matter not originally filed in the drawings, specifications and claims.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 22-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Park US Patent 5,902,127.

Park discloses the semiconductor apparatus as claimed. See figures 1A-5B, with emphasis on figures 4A-4E, and corresponding text where Park teaches an apparatus comprising: a substrate **40** (figure 4A; col. 4, lines 21-24); a barrier layer **44** over said substrate (figure 4A; col. 4, lines 24-29); a trench **46** etched into said substrate through said barrier (figure 4A; col. 4, lines 29-33); a dielectric **48/50** in said trench, said dielectric having a first etch rate (figures 4B-4C; col. 4, lines 34-47); and a plurality of ions implanted **Rp1** into said dielectric and said barrier layer, said substrate being substantially free of said ions, said implanted dielectric having an etch rate higher than said first etch rate (figure 4D; col. 4, lines 48-61).

Pertaining to claim 23, Park teaches the apparatus wherein the dielectric comprises silicon oxide (col. 4, lines 34-41).

Pertaining to claim 24, Park teaches the apparatus wherein said dielectric is damaged by said implanted ions (col. 4, lines 48-58, ***Note***: the Examiner considers it to be inherent that the dielectric is damaged by the plurality of implanted ions, since the implanted ions are within in the oxide layers).

Pertaining to claim 25, Park teaches the apparatus wherein said barrier layer is formed on nitride (col. 4, lines 23-25).

Pertaining to claim 26, Park teaches the apparatus wherein said ions are selected from the group consisting of silicon, carbon, nitrogen, and oxygen (col. 4, lines 48-54, nitrogen).

Pertaining to claim 27, Park teaches the apparatus wherein the upper surface of said barrier layer and said dielectric are coplanar (col. 4, lines 62-67; col. 5, lines 1-8, ***Note***: the Examiner takes the position that since the surface of the oxide layers are planarized using chemical mechanical polishing (CMP), and the barrier layer is later removed, it is inherent that the barrier layer and the dielectric are coplanar).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over He et al., US Patent 6,146,973 in view of Park US Patent 5,902,127.

He discloses the semiconductor method substantially as claimed. See figures 1-3, and corresponding text where, He shows pertaining to claim 1, an apparatus comprising: a substrate **10** (figure 1; col. 2, lines 16-20); a barrier layer **12** over said substrate (figure 1; col. 2, lines 20-26); a trench **14** etched into said substrate through said barrier layer (figure1; col. 2, lines 27-40); a dielectric **16** in said trench, said dielectric having a first etch rate (figure 2; col. 2, lines 41-48);

and a plurality of ions **22** implanted into said dielectric, said substrate being substantially free of said ions, said implanted dielectric having an etch rate higher than said first etch rate (figures 2 and 3; col. 2, lines 54-67; col. 3, lines 1-45). In addition, He shows, pertaining to claim 23, wherein the dielectric comprises silicon oxide (col. 2, lines 43-47). Also, He shows, pertaining to claim 24, wherein said dielectric is damaged by said implanted ions (figure 2; col. 3, lines 5-14). He shows, pertaining to claim 26, wherein said ions are selected from the group consisting of silicon, carbon, nitrogen and oxygen (col. 3, lines 12-13, silicon, nitrogen and oxygen). Finally, He shows, pertaining to claim 27, wherein the upper surface of said dielectric are coplanar (figure 3; col. 3, lies 40-45).

However, He fails to show, pertaining to claim 1, a plurality of ions implanted into said dielectric and said barrier. In addition, He fails to show, pertaining to claim 25, wherein said dielectric is formed of silicon nitride. Finally, He fails to show, pertaining to claim 27, wherein the upper surface of said barrier layer and said dielectric are coplanar.

Park teaches, in figures 4D, and corresponding text a similar technique that includes implanting into the dielectric and the barrier layer, where the barrier layer is a silicon nitride. In addition, Park teaches that the surface of the oxide layers are planarized using chemical mechanical polishing (CMP), and the barrier layer is later removed, as a result it is inherent that the barrier layer and the dielectric are coplanar (col. 4, lines 23-25, lines 62-67; col. 5, lines 1-8).

It would have been obvious to one of ordinary skill in the art to incorporate the following steps of: a plurality of ions implanted into said dielectric and said barrier; wherein said dielectric is formed of silicon nitride; wherein the upper surface of said barrier layer and said dielectric are coplanar, in the apparatus of He, pertaining to claims 1, 25 and 27, according to the combined

teachings of He and Park, with the motivation that, the implanted barrier layer as taught by Park, implies that it would be obvious to use a blanket ion implantation step in He, such that the barrier layer will include the implanted ions, for the purpose of protecting the substrate from damage due to the ion implantation process.

Response to Arguments

Applicant's arguments filed 8/29/05 have been fully considered but they are not persuasive. In response to the Remarks on pages 3and 4:

The Applicant raises the clear issue of whether Park suggest teaching exactly the opposite of where the implantation and its effects on the insulating layer and that there can be no reasonable conclusion except that the one cited instance is a typographical error.

Although, the limitations including an "etch rate" is regarded as new matter, the Examiner takes the position for the sake of *arguendo*, that Park does teach that the implanted dielectric layer will have a *higher etch rate* (with emphasis) and that there is no typographical error within the cited Park reference. Specifically, in col. 3, lines 35-40, Park teaches that the implanted nitrogen ions within the insulating layer can *increase the etch rate* (with emphasis) of the insulating layer, as a result, the insulating layer will have a higher etch rate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
December 8, 2005

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
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